Electronic Version
Stylesheet Version v1.1.1

[QUAD FLAT NO-LEAD CHIP CARRIER]

Abstract

A quad flat no-lead chip carrier for a wire-bonded chip package is provided. The chip carrier comprises a conductive plate, a plurality of conductive columns and a plurality of dielectric walls. A chip is attached to the conductive plate. The conductive plate furthermore has a plurality of columnar through holes distributed around a chip-bonding region. The conductive columns are set up within the columnar through holes. The dielectric walls are set up between the sidewall of the conductive columns and the inner surface of the columnar through holes. The chip is electrically connected to the conductive columns via conductive wires. The bottom end of the conductive columns serves as input/output contacts for connecting with external contacts. The chip carrier is able to increase overall density of the input/output contacts and improve the electrical performance of the chip package.